**September 9th Senior Project Meeting**

**Armstrong Hall 137 and 144: 4:00 – 5:15 P.M.**

**Members in Attendance:** All Members

**Next Week’s Work Plans:**

* **Zach**
  + Fix Schedule
  + RTR/RTS and XFC Protocol
  + Buying an FPGA and seeing if the school one will work
  + CORE for I2S Blocks
  + Start coding one of the I2S submodules (BIST Generator?)
* **Whitley**
  + Start coding the I2C module
  + CORE 9 for I2C Requirements
* **Julie**
  + EDA Tool Installation
  + Complete Register Block Documentation
  + Start coding the Register module
  + CORE 9 for Register Requirements
* **Kevin**
  + Complete one submodule for the I2S Block (Deserializer?)
  + Create test benches and test this submodule
  + CORE 9 for I2S Blocks
* **Dhruvit**
  + EDA Tool Installation
  + Start coding the Filter module
  + CORE 9 for the Filter module

**Meeting Notes:**

* The RTS/RTR and XFC protocols need to be in one place
  + Zach assigned as the owner to this
  + Should be finished by next Wednesday
* EDA Tools should be installed and a simple place and route test should be completed by next week
  + We will be downloading Mentor Tools
  + An action item is to contact by email or in person Mike about installing the tools
* Things that need to be added/changed for the Microsoft Project schedule
  + Creating test benches
  + Create test cases for individual blocks
  + Creating test cases
  + Correction: Microcontroller not “board” will be linked to the chip
  + Shorten the milestone names
  + Block level synthesis
  + Full chip simulation
* CORE requirements and use cases can be integrated to write test specifications
  + The new CORE license works
* Dr. Hernandez will give feedback on the schedule
* Dhruvit and Julie have access to 144-B
  + This is where we will be installing the EDA tools
  + Can we remotely connect to this computer-Ask Mike?
* Chip.v
  + Will instantiate everyone’s modules
  + We will need to create input/output submodules
* Create model in another environment that takes in the register states and inputs and produces the correct output
  + An end to end test case
  + This is used to verify that we are producing the correct outputs in our chip
  + Does not need to be the most sophisticated model due to time
* Test benches will be stored on the “tb” folder on GitHub
* FIFO will be very similar for all blocks
  + The only difference will be the size and the width
* Need to buy crystal oscillators (10, 20, or 100?)
* Whitley will do board design in spring semester
* PSoC configuration will take 1-2 weeks of time
  + Whitley may be assigned to this task